WHAT IS CLAIMED IS:

1. An image suppression filter circuit comprising:

a first phase shifter which receives an inphase input signal, and outputs a first output signal and a second output signal having a phase component substantially orthogonal to the first output signal;

a second phase shifter which receives a quadrature input signal having a phase component substantially orthogonal to the inphase input signal, and outputs a third output signal and a fourth output signal having a phase component orthogonal to the third output signal;

a first subtracter which subtracts the fourth output signal from the first output signal, and outputs a subtraction signal;

a first adder which adds the second output signal and the third output signal, and outputs an addition signal;

a third phase shifter which receives the subtraction signal, and outputs a fifth output signal having a second phase component as for the subtraction signal and a sixth output signal having a phase component orthogonal to the fifth output signal;

a fourth phase shifter which receives the addition signal, and outputs a seventh output signal having the second phase component as for the addition signal and an eighth output signal having a phase component

orthogonal to the seventh output signal;

a second subtracter which subtracts the eighth output signal from the fifth output signal, and outputs a subtraction result as an inphase output signal; and

a second adder which adds the sixth output signal and the seventh output signal, and outputs an addition result as a quadrature output signal.

2. An image suppression filter circuit according to claim 1, comprising a buffer device which inputs the first output signal and the fourth output signal respectively to the first subtracter, and a buffer device which input the second output signal and the third output signal respectively to the first adder.

3. An image suppression filter circuit according to claim 1, comprising a buffer device which inputs the fifth output signal and the eighth output signal to the second subtracter, and a buffer device which inputs the sixth output signal and the seventh output signal to the second adder.

4. An image suppression filter circuit according to claim 3, wherein the buffer device comprises a voltage current converter having a differential circuit structure, the second adder and the second subtracter add and subtract in a current mode, respectively.

5. An image suppression filter circuit according to claim 3, comprising a buffer device which inputs the first output signal and the fourth output signal to the

first subtracter, and a buffer device which inputs the second output signal and the third output signal to the first adder.

6. An image suppression filter circuit according to claim 5, wherein the buffer device comprises a voltage current converter having a differential structure, the adder and the subtracter operate in a current mode, respectively.

7. An image suppression filter circuit according to claim 1, wherein the first phase shifter and the second phase shifter have an identical circuit structure.

8. An image suppression filter circuit according to claim 1, wherein the third phase shifter and the fourth phase shifter have an identical circuit structure.

9. An image suppression filter circuit according to claim 1, wherein each of the first phase shifter, the second phase shifter, the third phase shifter and the fourth phase shifter comprises a bridge circuit including a first resistor, a first end connected to one end of the first resistor, a first capacitor having one end connected to the first end, a second end connected to the other end of the first capacitor, a second resistor having one end connected to the second end, a third end connected to the other end of the second resistor, a second capacitor having one end

connected to the third end, and a fourth end connected to the other end of the second capacitor and the fourth end being connected with the other end of the first resistor;

the first phase shifter receiving the inphase input signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the first output signal as potential of the third end of the bridge circuit and the second output signal as potential of the first end of the bridge circuit;

the second phase shifter receiving the quadrature input signal as a potential difference between the fourth end and the second end of the bridge circuit, and outputting the third output signal as potential of the third end of the bridge circuit and the fourth output signal as potential of the first end of the bridge circuit;

the third phase shifter receiving the subtraction signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the fifth output signal as potential of the third end of the bridge circuit and the sixth output signal as potential of the first end of the bridge circuit; and

the fourth phase shifter receiving the addition signal as potential difference between the fourth end

and the second end of the bridge circuit, and outputting the seventh output signal as potential of the third end of the bridge circuit and the eighth output signal as potential of the first end of the bridge circuit.

10. An image suppression filter circuit according to claim 1, wherein each of the first phase shifter, the second phase shifter, the third phase shifter and the fourth phase shifter comprises a bridge circuit including a first resistor, a first end connected to one end of the first resistor, a first capacitor having one end connected to the first end, a second end connected to the other end of the first capacitor, a second resistor having one end to be connected to the second end, a third end connected to the other end of the second resistor, a second capacitor having one end connected to the third end, and a fourth end connected to the other end of the second capacitor and the fourth end being connected with the other end of the first resistor;

the first phase shifter receiving the inphase input signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the first output signal as potential of the third end of the bridge circuit and the second output signal as potential of the first end of the bridge circuit;

the second phase shifter receiving the quadrature input signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the third output signal as potential of the third end of the bridge circuit and the fourth output signal as potential of the first end of the bridge circuit;

the third phase shifter receiving the subtraction signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the fifth output signal as potential difference between the third end and the first end of the bridge circuit and the sixth output signal as potential difference between the fourth end and the second end of the bridge circuit; and

the fourth phase shifter receiving the addition signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the seventh output signal as potential difference between the third end and the first end of the bridge circuit and the eighth output signal as potential difference between the fourth end and the second end of the bridge circuit.

11. An image suppression filter circuit according to claim 1, wherein each of the first phase shifter, the second phase shifter, the third phase shifter and the fourth phase shifter comprises a bridge circuit

including a first resistor, a first end connected to one end of the first resistor, a first capacitor having one end connected to the first end, a second end connected to the other end of the first capacitor, a second resistor having one end connected to the second end, a third end connected to the other end of the second resistor, a second capacitor having one end connected to the third end, and a fourth end connected to the other end of the second capacitor and the fourth end being connected with the other end of the first resistor;

the first phase shifter receiving the inphase input signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the first output signal as potential difference between the third end and the first end of the bridge circuit and the second output signal as potential difference between the fourth end and the second end of the bridge circuit;

the second phase shifter receiving the quadrature input signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the third output signal as potential difference between the third end and the first end of the bridge circuit and the fourth output signal as potential difference between the fourth end and the second end of the bridge circuit;

the third phase shifter receiving the subtraction signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the fifth output signal as potential of the third end of the bridge circuit and the sixth output signal as potential of the first end of the bridge circuit; and

the fourth phase shifter receiving the addition signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the seventh output signal as potential of the third end of the bridge circuit and the eighth output signal as potential of the first end of the bridge circuit.

12. An image suppression filter circuit according to claim 1, wherein the first phase shifter, the second phase shifter, the third phase shifter and the fourth phase shifter are respectively constituted of a bridge circuit including a first resistor, a first end connected to one end of the first resistor, a first capacitor having one end connected to the first end, a second end connected to the other end of the first capacitor, a second resistor having one end connected to the second end, a third end connected to the other end of the second resistor, a second capacitor having one end connected to the third end, and a fourth end connected to the other end of the second capacitor and

the fourth end being connected with the other end of the first resistor;

the first phase shifter receiving the inphase input signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the first output signal as potential difference between the third end and the first end of the bridge circuit and the second output signal as potential difference between the fourth end and the second end of the bridge circuit;

the second phase shifter receiving the quadrature input signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the third output signal as potential difference between the third end and the first end of the bridge circuit and the fourth output signal is output as potential difference between the fourth end and the second end of the bridge circuit;

the third phase shifter receiving the subtraction signal as potential difference between the fourth end and the second end of the bridge circuit, outputting the fifth output signal as potential difference between the third end and the first end of the bridge circuit and the sixth output signal is output as potential difference between the fourth end and the second end of the bridge circuit; and

the fourth phase shifter receiving the addition

signal as potential difference between the fourth end and the second end of the bridge circuit, and outputting the seventh output signal as potential difference between the third end and the first end of the bridge circuit and the eighth output signal is output as potential difference between the fourth end and the second end of the bridge circuit.

13. An image suppression filter circuit comprising:

a pre-stage phase shifter; and

a plurality of rear-stage phase shifters;

the pre-stage phase shifter including:

a first phase shifter which receives an inphase input signal, and outputs a first output signal and a second output signal having a phase component substantially orthogonal to the first output signal;

a second phase shifter which receives a quadrature input signal having a phase component substantially orthogonal to the inphase input signal, and outputs a third output signal and a fourth output signal having a phase component orthogonal to the third output signal;

a first subtracter which subtracts the fourth output signal from the first output signal, and outputs a subtraction signal; and

a first adder which adds the second output signal and the third output signal, and outputs an addition signal; and

each of the rear-stage phase shifter including:

a third phase shifter which receives the subtraction signal, and outputs a fifth output signal having a second phase component as for the subtraction signal and a sixth output signal having a phase component orthogonal to the fifth output signal;

a fourth phase shifter which receives the addition signal, and outputs a seventh output signal having the second phase component as for the addition signal and an eighth output signal having a phase component orthogonal to the seventh output signal;

a second subtracter which subtracts the eighth output signal from the fifth output signal, and outputs a subtraction result as an inphase output signal; and

a second adder which adds the sixth output signal and the seventh output signal, and outputs an addition result as a quadrature output signal.

14. An image suppression filter circuit according to claim 13, comprising a buffer device which receives the first output signal and the fourth output signal respectively to the first subtracter, and the second output signal and the third output signal respectively to the first adder.

15. An image suppression filter circuit according to claim 13, comprising a buffer device which inputs the fifth output signal and the eighth output signal to the second subtracter, and the sixth output signal and

the seventh output signal to the second adder.

16. An image suppression filter circuit according to claim 13, wherein the first phase shifter and the second phase shifter have an identical circuit structure.

17. An image suppression filter circuit according to claim 13, wherein the third phase shifter and the fourth phase shifter have an identical circuit structure.

18. A receiver apparatus comprising:

an amplifier which amplifies an input signal to output an amplified signal;

an input side mixer which receives the amplified signal and outputs an inphase signal having a phase component inphase with the amplified signal and a quadrature signal having a phase component orthogonal to the first signal;

an image suppression filter circuit according to claim 1 and configured to receive a first signal corresponding to the inphase signal and a second signal corresponding to the quadrature signal and output an inphase output signal;

an output side mixer which converts the inphase output signal from the image suppression filter circuit into an inphase reception signal and a quadrature reception signal.

19. A transmitter apparatus comprising:

a first quadrature modulator which converts a transmission inphase signal and a transmission quadrature signal into an intermediate frequency signal;

an image suppression filter circuit according to claim 1 and configured to generate an inphase output signal and a quadratur output signal based on the intermediate frequency signal, the inphase output signal and the quadrature output signal being different in phase by 90 degrees from each other; and

a second quadrature modulator which converts the inphase output signal and the quadrature output signal into a radio frequency signal.